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Implementation of FM0/Manchester Encoding and Systematic Codes on FPGA

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Abstract: Software Defined Radio (SDR) is an emerging technology to realize the many applications without using different hardware components. The FM0/Manchester and systematic codes can be combined to achieve high throughput.FM0/Manchester codes can be used to reach the dc balance and enhancing signal reliability. Systematic codes are used to detect and correct the errors. In this code, the code input is embedded into the encoded output. BWA architecture is used in systematic codes, which is implemented using parallel processing unit to achieve high speed. These encoding techniques are combined using mode selection signal. SOLS technique can be used to reduce the number of transistor used in the architecture. This combined architecture can be implemented in VHDL coding using MODELSIM SE 6.2C software. This proposed architecture can be verified using the FPGA (SPARTAN 3E) kit. An experimental result shows less area and high throughput.

Keywords: FM0, Manchester, Software Defined Radio (SDR), Systematic codes, Similarity Oriented Logic Simplification (SOLS), Butter-fly Formed Weighted Accumulator (BWA), Field Programmable Gate Array (FPGA).

I. INTRODUCTION

In this paper, we have proposed a combined architecture of systematic codes and FM0/Manchester codes for Software Defined Radio (SDR) application. Software Defined Radio is defined as Radio in which some or all of the physical layer functions are software defined. SDR is a radio communication system where components that have implemented in a hardware (ex: mixer, filters, detectors) are instead implemented using a software on personal computer or embedded systems. It refers to the technology wherein software modules running on a generic hardware platform consisting of DSPs and general purpose microprocessors are used to implement radio functions such as generation of transmitted signal (modulation) at transmitter and tuning/detection of received radio signal (demodulation) at receiver. These SDR plat form consist of three parts: RF section, IF section, Baseband section. RF section is used to transmit and receive the wireless signal through antenna. Baseband section is used for modulation, encoding, clock synchronization purposes. The IF section is used for conversion purposes consist of four blocks such as ADC, DAC, DUC, DDC.

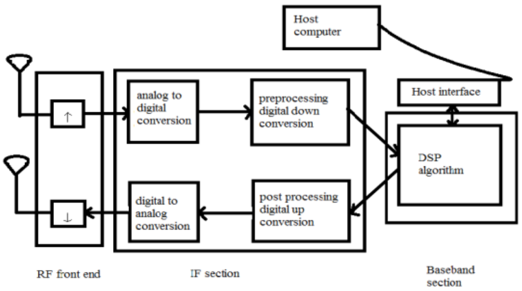
Host computer
Host interface
analog to digital conversion
preprocessing digital down conversion
DSP algorithm
digital to analog conversion
post processing digital up conversion
↑
↓
RF front end
IF section
Baseband section

Fig 1: Architecture of SDR transceiver

The baseband section performs the modulation methods such as amplitude shift keying, phase shift keying, frequency division multiplexing. The transmitted signal having binary sequence, so it does not reach the DC balance. Data encoding like FM0 and Manchester code is used to provide the DC balance. The coding diversity between the FM0 and Manchester limits the potential to design the VLSI architecture. Systematic codes are error correcting codes consisting of raws of data and parity information in systematic form generated by the encoding. It is used to reduce the latency and complexity of hardware architecture. Error correcting codes are also used to protect the data and to improve the reliability.

So we use Similarity Oriented Logic Simplification (SOLS) technique to create reusable VLSI architecture. It consists of two methods: area compact retiming and balance logic operation sharing. Area compact retiming process is used to reduce the number of transistors used in the architecture. Balance logic operation sharing is used to combine the codes used in the architecture.

II. PREVIOUS WORKS

1. The literature [4] proposes VLSI architecture combines frequency shift keying modulation and demodulation using Manchester code for hardware realisation. It is used for SDR application.
2. The literature [5] proposes a high speed fully reused VLSI architecture for RFID application using FM0 and Manchester encoding.
3. The literature [6] proposes VLSI architecture achieves less data rate when compared to Japan DSRC standard. Area can be reduced using the SOLS technique.
4. The literature [7] proposes a Manchester encoding architecture for UHF RFID Tag emulator. It is

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realised into Field-Programmable Gate Array (FPGA) prototyping system. It does not maintain a stable DC performance.

5. The literature [9] proposes a fully reused VLSI architecture for FM0 and Manchester codes using SOLS technique. SOLS technique is used to reduce the number of transistor used in architecture and it combines FM0 and Manchester codes. It improves hardware utilization from 51.7% to 100%.

III. PRINCIPLES OF FM0, MANCHESTER AND SYSTEMATIC CODES

In this section, the clock signal and the input data can be represented as CLK and X. The coding principles of FM0 and Manchester is described as follows,

A.FM0 Encoding

FM0 code consist of two parts: one for former-half cycle of CLK, A, and the other later-half cycle of CLK, B. It consist of three rules,

1. If X is logic-0, code exhibits the transition between A and B.
2. If X is logic-1, code does not exhibit the transition between A and B.
3. The transition is allocated among the each FM0 code no matter what X is.

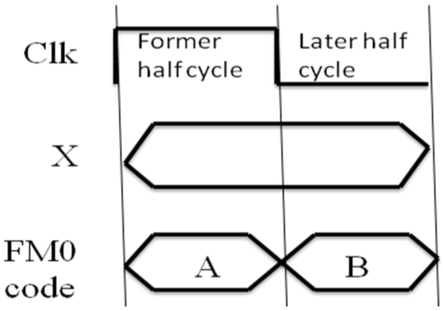

Fig 2: Illustration of FM0 code based on above three rules.

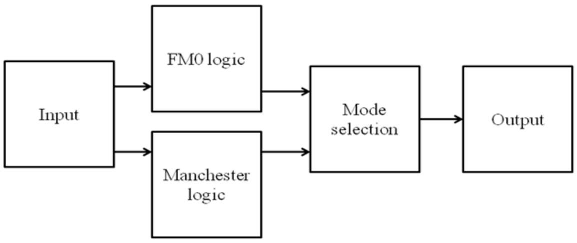

Fig 3: Block diagram of FM0/Manchester codes.

B. Manchester Encoding

In Manchester encoding 0 and 1 bit are represented in a clock cycle by the signals. Here the signal transitions are occurs in the middle of the cycle. The Manchester code is derived from

$$X \oplus CLK.$$

The Manchester encoding is performed with a XOR operation for CLK and X. The clock always has a transition within one cycle and so does the Manchester code irrespective to what the X is.

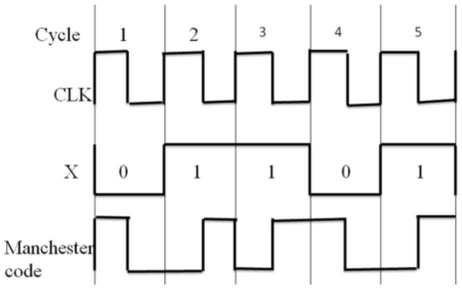

Fig 4: Illustration of Manchester code based on above rules.

C. Systematic codes

Systematic codes can be used to calculate the hamming distance (ex: minimum distance).for systematic linear codes, the generator matrix G is represented as,

$$G= [I_k | P]$$

Where I_k is identity matrix.

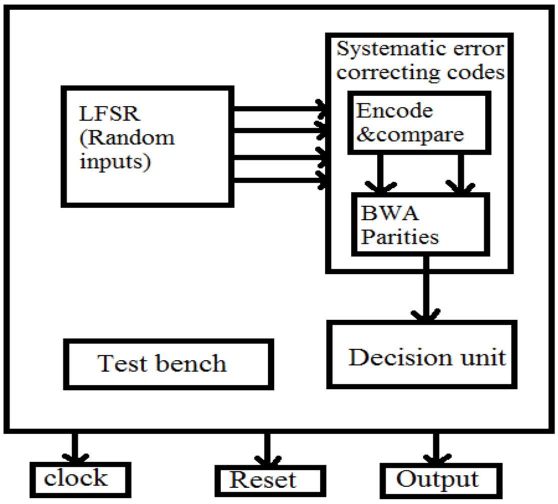

Fig 5:Block diagram of systematic codes.

IV. BLOCK DIAGRAM

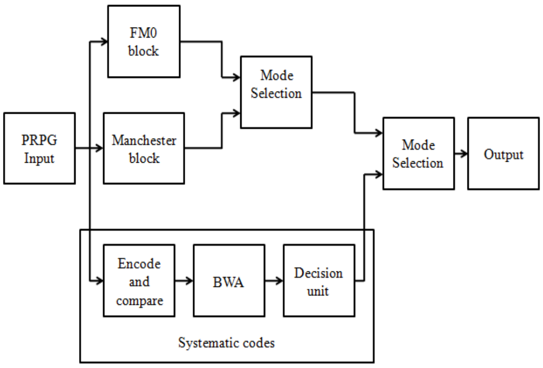

Fig 6: Block diagram of proposed method

A.BLOCK DIAGRAM EXPLANATION

A. Overview:

The block diagram uses five main blocks such as random generator, FM0 block, Manchester block, systematic code block and mode selection. The Linear Feedback Shift Register act as a pseudo random pattern generator to

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generate a random inputs and it is given to the three code block. Systematic code block consist of three sub blocks such as encoding and comparison, BWA block and decision unit. The incoming bits can be encoded using three encoding architecture.FM0/Manchester output can be selected as a output using mode selection signal. In systematic codes encode and Compare block can be used to encode the input bits and then it is made comparison performed on encoded output and the incoming bits to detect the error. BWA is used to store the data bits and parities separately. Decision unit is used to make the decision such as match, mismatch and fault. Another mode selection operation can be performed on systematic codes and FM0/Manchester codes. Test bench is used to observe the experimental results.

B. Pseudo Random Pattern Generator
LFSR is used to give the input patterns to circuit. Retrieved code word and incoming tags are generated by the random generator. It is an algorithm for generating a sequence of numbers whose properties approximate the properties of sequences of random number.

C.FM0 block
Frequency modulation 0 depends not only on the PRPG input both of the previous state output. Consider logic 0 as a input, phase inversion can be occurred in the output.

D.Manchester Block
It performs the XOR operation between the PRPG input and the clock signal.

E. Encode and Compare architecture
A k-bit input bits are encoded corresponding to the n-bit code word X and the codeword X is compared with the n-bit retrieved codeword Y. Fig. 7 represents the Encode and Compare architecture. The comparison is used to fine the how many number of bits can differ in the codeword X and Y (i.e. Hamming Distance).Hamming distance can be represented as “d”.

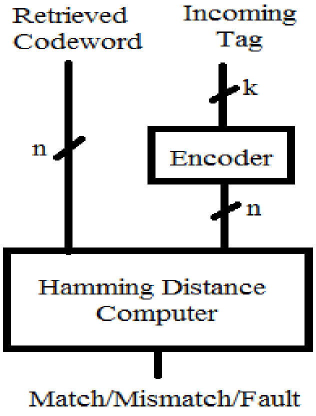

Fig 7: Encode and Compare architecture.

F. BWA architecture
Butter-fly Formed Weighted Accumulator is used to reduce the latency and complexity of the minimum distance (i.e. Hamming distance).BWA stores the data bits separately. For ex, Half Adder produces two outputs such as sum and carry bit which are stored separately.

G. Test bench
Test bench is referred as testing environment or testing workbench. It is a virtual environment used to verify the correctness or design or circuit model. Ex: Software product. The tools used to automate the testing process in a test bench perform some functions such as test data generator, test manager, report generator, file comparator, dynamic analyser, etc.

V. HARDWARE ARCHITECTURE OF FM0, MANCHESTER AND SYSTEMATIC CODES

A. Architecture for FM0 and Manchester code
First, we realise the architecture of FM0 and Manchester codes. The red dashed line represents the FM0 logic and the blue dashed line represents the Manchester logic. The FM0 logic depends on the data input X and the previous state of the code. DFF_A and DFF_B are used to store the state of the FM0 code. The MUX-1 is used for switching operation A(t) and B(t) using clock signal. The Manchester code performs simple XOR operation between X and clock signal, CLK. the MUX-2 is used for Mode selection purpose. The Mode 0 is used for FM0 code and the Mode 1 is used for Manchester code. These codes are used to evaluate the Hardware Utilisation Rate (HUR).

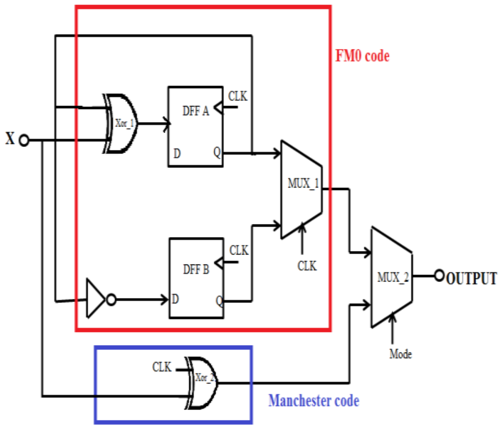

Fig 8: FM0 and Manchester architecture.

The SOLS technique is used to design fully reused VLSI architecture for FM0 and Manchester code. SOLS consist of two methods: area compact retiming and the balance logic operation sharing. Area compact retiming is used to reduce the number of transistor used in the architecture. Balance logic operation sharing is used for combining the FM0 and Manchester codes. This can be realised using the multiplexer. The various logic families can be used to realise the logic functions of SOLS techniques. Electrical performance such as area, power can be optimised using the logic families.

B. Architecture for systematic codes
The architecture fig. 9 represents for computing the hamming distance. This architecture contains multiple BWA to reduce the latency and complexity of computing

the hamming distance.BWA is used to count the number of 1's present in the input bits. A k-bit incoming tag is encoded using the n-bit codeword X and then the encoded output is compared to the n-bit retrieved code word. Hamming distance can be calculated to detect the errors. Hamming distance can be calculated using four conditions:

1) If d=0, the input X and the output Y will match exactly.
2) If 0<d<= t_{max} means input X will match the output Y are corrected.
3) If t_{max}<d<=r_{max} means input Y has detectable, but the detectable error does not corrected.
4) r_{max}<d means the input X does not match the output Y.

XOR bank is used to generate a vector of bitwise difference of two code words. The P_{max} gives the two information such as r_{max} and t_{max}. The r_{max} represents the number of maximally detectable errors and t_{max} represents the number of maximally correctable errors.

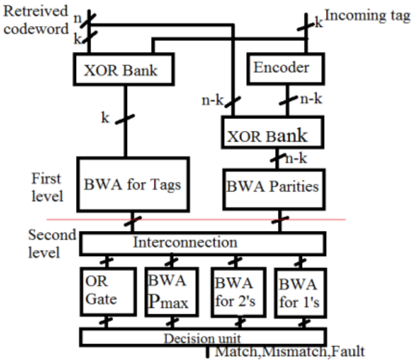

Fig 9: Architecture optimized for systematic code words

C.parallel processing architecture for BWA

Consider a Fig 10, Simple (8, 4) error correction and error detection code. The circuit contains multiple half adders which are associated with the weight 1, 2 and 4.the encoder and XOR bank is not used in Fig 8, for simplicity. The bit consist of weight 4 are ORed together. The bit consist of weight 2 is for 2's complement and the bit consist of weight 1 is for 1's complement.

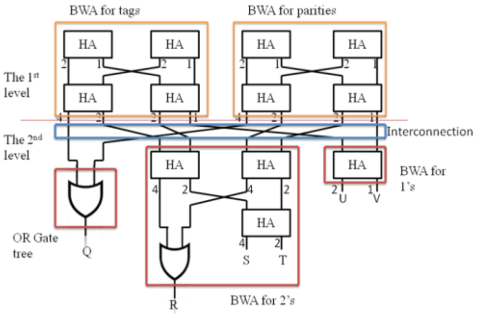

Fig 10: Parallel processing architecture for BWA.

The output of the BWA for OR gate, BWA for 2's complement, BWA for 1's complement and BWA for Pmax are given to the decision unit. Decision unit is used to make the decision such as match, mismatch and fault using the truth table.

TABLE I: TRUTH TABLE OF THE DECISION UNIT FOR (8, 4) CODE

Q or R or S	T	U	V	Decision
0	0	0	X	Match
	0	1	X	Fault
	1	0	0	Fault
	1	0	1	Mismatch
	1	1	X	Mismatch
1	X	X	X	Mismatch

Table I represents the truth table of decision unit. The output of the decision unit is to determine the incoming tag X matches the retrieved code word Y using the four ranges of hamming distance. The U and V, both cannot be set simultaneously, these term can be included in don't care terms.

VI. EXPERIMENTAL RESULTS AND DISCUSSION

The simulation can be done using the MODELSIM6.2c. fig 11 represents the simulation result for Fm0 and Manchester code. The linear feedback shift register produces the random inputs which are coded using the principle of FM0 and Manchester codes. The coding can be written using the VHDL language. The waveform can be verified by using test bench. The simulation result can be obtained to such a way that the design of architecture that they act as either in FM0 and Manchester code.

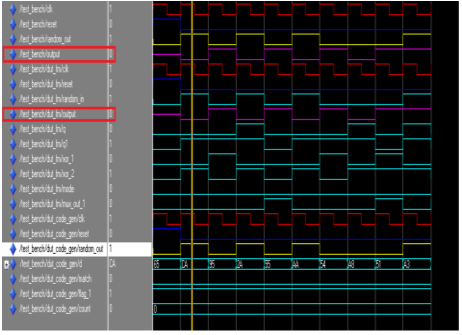

Fig 11: Simulation result for FM0 and Manchester code

Fig 12 represents the simulation result for systematic codes. In this code LFSR is used to generate the input patterns and encoding can be done then the output is compared to the input to detect and correct the errors easily. This can be verified using the test bench waveform. This systematic code reduces the latency and hardware complexity of architecture. It is also used to improve throughput.

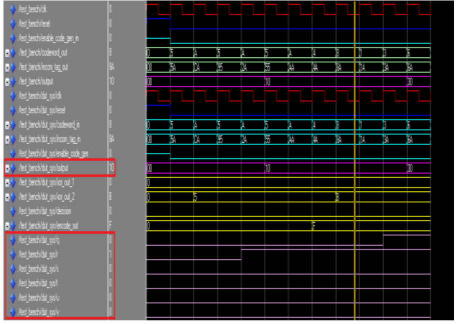

Fig 12: Simulation result for systematic codes

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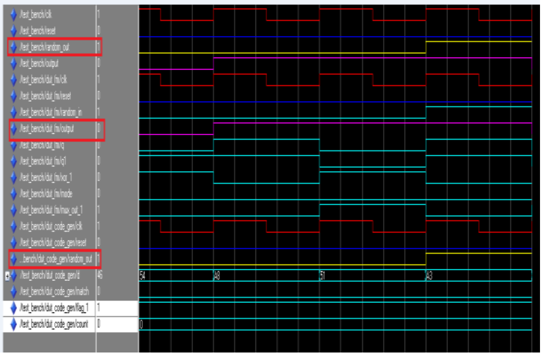
Fig 13 represents the simulation result for combined codes. The linear feedback shift register produces the random inputs which are coded using the principle of FM0, Manchester and systematic codes. The coding can be written using the VHDL language. The waveform can be verified by using test bench. The simulation result can be obtained to such a way that the design of architecture that they act as either in FM0, Manchester and systematic code.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/test_bench/reset 0
/test_bench/random_out 1
/test_bench/output 0
/test_bench/dut_fm/clk 1
/test_bench/dut_fm/reset 0
/test_bench/dut_fm/random_in 1
/test_bench/dut_fm/output 0
/test_bench/dut_fm/q 0
/test_bench/dut_fm/q1 0
/test_bench/dut_fm/xor_1 0
/test_bench/dut_fm/mode 0
/test_bench/dut_fm/mux_out_1 1
/test_bench/dut_code_gen/clk 1
/test_bench/dut_code_gen/reset 0
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/test_bench/dut_code_gen/d 46
/test_bench/dut_code_gen/match 0
/test_bench/dut_code_gen/flag_1 1
/test_bench/dut_code_gen/count 0
54
0

Fig 13: Simulation result for combined codes such as FM0/Manchester and Systematic codes.

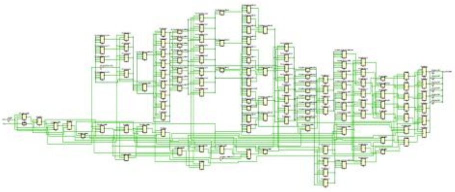

Fig 14: RTL schematic of combined architecture.

	FM0/ MANCHESTER	SYSTEMATIC CODE	COMBINED
Number of Slice Flip Flop	7	95	95
Number of Slices	4	75	62
LUTs	4	114	113
Throughput	34.14 MBPS	36.65 MBPS	42.86 MBPS

Fig 15: comparison table of area and throughput.

VII. CONCLUSIONS

In this project, fully reused VLSI architecture can be designed using FM0, Manchester and the Systematic codes. The parallel operation is performed based on the systematic codeword has separate field for data and parity. The proposed combined architecture is used to reduce the complexity to find the errors and correct the errors. In this architecture, mode selection process is used to select the code such as either FM0/Manchester or systematic code. In SDR application, modulation changes, the codes for error correction and detection can be changed. This code matches the incoming data to the stored data if the erroneous bits are corrected. The test bench waveform can be analysed using the modelsim6.2c. It is implemented in Spartan 3E FPGA kit using Xilinx synthesis code. It gives high throughput compared to the existing articles. This paper not only considers reducing power consumption it also achieves the less area. So these coding techniques are efficient. The proposed method is used for diverse application.

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